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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
MILORD, MARCEAU	
ART UNIT	**PAPER NUMBER**
2618	

DATE MAILED: 05/16/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,252	KOMAILI ET AL.	
	Examiner	Art Unit	
	Marceau Milord	2618	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kiyanagi et al (US Patent No 6185201 B1) in view of Borras et al (US Patent No4394776).

Regarding claims 1-3, 6-9, Kiyanagi et al discloses a system for synchronizing a portable transceiver to a network (figs. 1, 16-17), comprising: a crystal oscillator; a frequency synthesizer adapted to receive an output of the crystal oscillator (col. 24, lines 40-67; col. 25, lines 16-47); logic coupled to the crystal oscillator, the logic configured to estimate a frequency error of a received signal (col. 28, lines 31-55; col. 33, lines 12-55).

However, Kiyanagi et al does not specifically disclose the feature of a first control signal supplied from the logic to the frequency synthesizer, the first control signal configured to adjust the frequency synthesizer to compensate for the error; and a second control signal supplied from the logic to the tuning circuitry, the second control signal configured to adjust the tuning

circuitry, the tuning circuitry configured to compensate for the error; wherein the adjustment of the frequency synthesizer adjusts the timing of the portable transceiver with respect to a communication network.

On the other hand, Borras et al, from the same field of endeavor, discloses a frequency-synthesized transceiver capable of tuning to a plurality of communication channels. The transceiver includes a receiver section and a transmitter section, which is coupled to the synthesizer, which generates the appropriate injection, signals to achieve tuning. The frequency synthesizer includes a multiposition switch which accesses various addressable memory locations in a programmable read-only memory where the appropriate divisors are stored to cause tuning of the synthesizer to the appropriate communication channel. The synthesizer includes a priority channel monitoring system utilizing a channel element for rapid sampling. The divisors are supplied to a single synchronous binary swallow counter which works in conjunction with a dual modulus prescaler to monitor the frequency output of the voltage controlled oscillator (col. 3, lines 40-57). A programmable divider coupled to a reference oscillator source is compared with the output of the synchronous counter in a digital and analog phase detector. The phase detector supplies signals through a loop filter to apply the appropriate voltage to the voltage-controlled oscillator. The phase detector includes means to rapid advance the voltage-controlled oscillator to cause frequency tuning (col. 5, lines 27-43; col. 6, lines 44-61). Furthermore, the output of transmitter phase detector is coupled to a transmitter lock detector, which has a first output coupled to PLL interface gate and a second output coupled to sweep control. The output of sweep control is coupled to error signal circuit, which also receives an input directly from the phase detector. The output of error signal circuit is coupled to a

transmitter VCO which has a first output coupled back to phase detector. The modulated information is supplied to transmitter phase detector, which, supplies information both to transmitter error signal detector and transmitter lock detector. The output of transmitter error signal is coupled to transmitter VCO that also supplies a signal back to transmitter phase detector (col. 10, lines 8-24; col. 10, lines 59-66). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Borras to the communication system of Kiyanagi in order to provide a digital frequency synthesized transceiver system for portable transceivers which will provide the size reduction, power conservation and programmability that a multiple of users require.

Claim 4 contains similar limitations addressed in claims 1-3, and therefore are rejected under a similar rationale.

Regarding claim 5, Kiyanagi et al as modified discloses a system for synchronizing a portable transceiver to a network (figs. 1, 16-17), wherein the tuning circuitry comprises a digital-to-analog converter (col. 3, lines 46-57; col. 7, lines 62- col. 8, line 12).

Regarding claims 10-13, 15-18, Kiyanagi et al discloses a method for synchronizing a portable transceiver to a network (figs. 1, 16-17), comprising: determining a

frequency error of a signal received by the portable transceiver (col. 24, lines 40-67; col. 25, lines 16-47).

However, Kiyanagi et al does not specifically disclose the step of adjusting the frequency of the system by adjusting a frequency synthesizer to compensate for the error if the frequency error is less than a predetermined value; wherein the adjustment of the frequency synthesizer adjusts the timing of the portable transceiver with respect to a communication network.

On the other hand, Borras et al, from the same field of endeavor, discloses a frequency-synthesized transceiver capable of tuning to a plurality of communication channels. The transceiver includes a receiver section and a transmitter section, which is coupled to the synthesizer, which generates the appropriate injection, signals to achieve tuning. The frequency synthesizer includes a multiposition switch which accesses various addressable memory locations in a programmable read-only memory where the appropriate divisors are stored to cause tuning of the synthesizer to the appropriate communication channel. The synthesizer includes a priority channel monitoring system utilizing a channel element for rapid sampling. The divisors are supplied to a single synchronous binary swallow counter which works in conjunction with a dual modulus prescaler to monitor the frequency output of the voltage controlled oscillator (col. 3, lines 40-57). A programmable divider coupled to a reference oscillator source is compared with the output of the synchronous counter in a digital and analog phase detector. The phase detector supplies signals through a loop filter to apply the appropriate

voltage to the voltage-controlled oscillator. The phase detector includes means to rapid advance the voltage-controlled oscillator to cause frequency tuning (col. 5, lines 27-43; col. 6, lines 44-61). Furthermore, the output of transmitter phase detector is coupled to a transmitter lock detector, which has a first output coupled to PLL interface gate and a second output coupled to sweep control. The output of sweep control is coupled to error signal circuit, which also receives an input directly from the phase detector. The output of error signal circuit is coupled to a transmitter VCO which has a first output coupled back to phase detector. The modulated information is supplied to transmitter phase detector, which, supplies information both to transmitter error signal detector and transmitter lock detector. The output of transmitter error signal is coupled to transmitter VCO that also supplies a signal back to transmitter phase detector (col. 10, lines 8-24; col. 10, lines 59-66). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Borras to the communication system of Kiyanagi in order to provide a digital frequency synthesized transceiver system for portable transceivers which will provide the size reduction, power conservation and programmability that a multiple of users require.

Regarding claim 14, Kiyanagi et al as modified discloses a method for synchronizing a portable transceiver to a network (figs. 1, 16-17) further comprising using a digital-to-analog converter to adjust the frequency of the crystal oscillator (col. 3, lines 46-57; col. 7, lines 62- col. 8, line 12).

Regarding claims 19-22, 24-27, Kiyanagi et al discloses a system for synchronizing a portable transceiver to a network (figs. 1, 16-17), comprising: means for determining a frequency error of a signal received by the portable transceiver (col. 24, lines 40-67; col. 25, lines 16-47).

However, Kiyanagi et al does not specifically disclose the feature of a means for adjusting the frequency of the system by adjusting a frequency synthesizer to compensate for the error if the frequency error is less than a predetermined value; wherein the adjustment of the frequency synthesizer adjusts the timing of the portable transceiver with respect to a communication network

On the other hand, Borras et al, from the same field of endeavor, discloses a frequency-synthesized transceiver capable of tuning to a plurality of communication channels. The transceiver includes a receiver section and a transmitter section, which is coupled to the synthesizer, which generates the appropriate injection, signals to achieve tuning. The frequency synthesizer includes a multiposition switch which accesses various addressable memory locations in a programmable read-only memory where the appropriate divisors are stored to cause tuning of the synthesizer to the appropriate communication channel. The synthesizer includes a priority channel monitoring system utilizing a channel element for rapid sampling. The divisors are supplied to a single synchronous binary swallow counter which works in conjunction with a dual modulus prescaler to monitor the frequency output of the voltage

controlled oscillator (col. 3, lines 40-57). A programmable divider coupled to a reference oscillator source is compared with the output of the synchronous counter in a digital and analog phase detector. The phase detector supplies signals through a loop filter to apply the appropriate voltage to the voltage-controlled oscillator. The phase detector includes means to rapid advance the voltage-controlled oscillator to cause frequency tuning (col. 5, lines 27-43; col. 6, lines 44-61). Furthermore, the output of transmitter phase detector is coupled to a transmitter lock detector, which has a first output coupled to PLL interface gate and a second output coupled to sweep control. The output of sweep control is coupled to error signal circuit, which also receives an input directly from the phase detector. The output of error signal circuit is coupled to a transmitter VCO which has a first output coupled back to phase detector. The modulated information is supplied to transmitter phase detector, which, supplies information both to transmitter error signal detector and transmitter lock detector. The output of transmitter error signal is coupled to transmitter VCO that also supplies a signal back to transmitter phase detector (col. 10, lines 8-24; col. 10, lines 59-66). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to apply the technique of Borras to the communication system of Kiyanagi in order to provide a digital frequency synthesized transceiver system for portable transceivers which will provide the size reduction, power conservation and programmability that a multiple of users require.

20. The system of claim 19, further comprising: means for adjusting the frequency of the crystal oscillator by adjusting a tuning circuit associated with the crystal oscillator.

Regarding claim 23, Kiyanagi et al as modified discloses a system for synchronizing a portable transceiver to a network (figs. 1, 16-17), wherein the means for adjusting the frequency of the crystal oscillator comprises a digital-to-analog converter (col. 3, lines 46-57; col. 7, lines 62- col. 8, line 12).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Borras et al discloses a frequency-synthesized transceiver capable of tuning to a plurality of communication channels.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marceau Milord whose telephone number is 571-272-7853. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew D. Anderson can be reached on 571-272-4177. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MARCEAU MILORD

Marceau Milord
Primary Examiner
Art Unit 2618

5-10-06